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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,478	02/26/2004	Gerald Keith Bartley	ROC920030354US1	6994

7590 09/28/2005

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EXAMINER	
GARLAND, STEVEN R	

ART UNIT	PAPER NUMBER
2125	

DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,478	BARTLEY ET AL.	
	Examiner	Art Unit	
	Steven R. Garland	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-18* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 are pending.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1,2,4-7,10-12, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schettler et al. EPO 0417345 in view of Yamamichi et al. 6,524,905 .

Schettler teaches system design of a passive silicon carrier 3 and chip 1,2 combination. Schettler also teaches that it is desirable to design the chips and package carrier together so as to reduce complexity. Schettler also provides decoupling capacitors (col. 3 line 22) and use of the flip chip technique (col. 6, lines 10-17). Schettler also teaches multi-chip design on a Silicon carrier in figs. 5 and 6.

See the abstract; figures; col. 1, lines 1-15 and 43-58; col. 3, lines 10-22; col. 4, lines 4-28; col. 5, line 13 to col. 6, line 35. Note figure 1 shows an implemented physical design with a selected number of chips having various parameters and the capacitors have a selected size, shape, and number of connections..

Schettler however does not specifically state that a system is used to generate the physical design and assemble the components.

Yamamichi teaches a design system which receives an order for a circuit including a decoupling capacitor and designs a circuit and decoupling capacitor with associated packaging all subject to the customer's order requirements including pricing. Yamamichi also teaches mounting the elements on the packaging. See figures 11-12 and col. 11, line 58 to col. 12, line 36.

It would have been obvious to one of ordinary skill in the art to modify Schettler in view of Yamamichi and use such a design system to generate the physical design of the carrier and chip arrangement of Schettler and also to assemble the components.

5. Claim 3, 8,9, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schettler et al. EPO 0417345 in view of Yamamichi et al. 6,524,905 as applied to claims 1,2,4-7,10-12, and 15-18 above, and further in view of Chudzik et al. 2004/0108587.

Schettler teaches system design of a passive silicon carrier 3 and chip 1,2 arrangement. Schettler also teaches that it is desirable to design the chips and packages together so as to reduce complexity. Schettler also provides decoupling capacitors (col. 3 line 22) and use of the flip chip technique. See the abstract; figures;

col. 1, lines 1-15 and 43-58; col. 3, lines 10-22; col. 4, lines 4-28; col. 5, line 13 to col. 6, line 35. Note figure 1 shows an implemented physical design with a selected number of chips and the capacitors have a selected size and shape.

Schettler however does not specifically state that a system is used to generate the physical design and assemble the components.

Yamamichi teaches a design system which receives an order for a circuit including a decoupling capacitor and designs a circuit and decoupling capacitor with associated packaging all subject to the customer's order requirements including pricing. Yamamichi also teaches mounting the elements on the packaging. See figures 11-12 and col. 11, line 58 to col. 12, line 36.

It would have been obvious to one of ordinary skill in the art to modify Schettler in view of Yamamichi and use such a design system to generate the physical design of the carrier and chip arrangement of Schettler and also to assemble the components.

Schettler and Yamamichi however do not teach the use of passive resistors on the silicon carrier.

Chudzik et al. teaches the use of passive capacitors and passive resistors decoupling elements on a silicon carrier to reduce switching noise of power at high frequencies. See the abstract; figures; paragraphs 0002,0004-0008; 0025,0026,0029,0032,0035, and 0041.

It would have been obvious to one of ordinary skill in the art to modify Schettler and Yamamichi in view of Chudzik and use both passive capacitors and resistors on the

silicon substrate to further reduce noise at the selected frequency range and power range.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nassif et al. 6,898,769 and Becker et al. 2005/0108671 are of interest in the use of decoupling capacitors and package design.

7. Claim 14 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven R. Garland whose telephone number is 571-272-3741. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven R Garland

Examiner
Art Unit 2125

9/21/05

Albert W. Paladini 9-26-05
ALBERT W. PALADINI
PRIMARY EXAMINER